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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,444	10/07/2003	Nang-Ping Chen		4481

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EXAMINER	
JACOB, MARY C	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,444	CHEN ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 92. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

4. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

5. The Abstract, line 21, “signal” should read, “signals”.

Claim Objections

6. Claims 6 and 11 are objected to because of the following informalities. Appropriate correction is required.

7. Claim 6, line 2, “array” is spelled incorrectly.

8. Claim 11, step iii recites “the circuit or system emulated”, it would be better if written, “the electronic circuit or system emulated”.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 1 recites “an electronic circuit” in line 6 and “a circuit” in line 7. It is unclear if these limitations refer to the same “circuit” or if “an electronic circuit” and “a circuit” are intended to be two separate circuits.

12. Claim 2, line 7 and Claim 11, line 13 recite the limitation "the limits". There is insufficient antecedent basis for this limitation in the claims.

13. Claim 3 recites, "the circuit" in lines 1 and 9. It is unclear as to whether the limitation of "the circuit" in this claim refers to "a circuit" claim 1, line 7, or "an electronic circuit" referred to in claim 1, line 6 and claim 2, line 5.

14. Claims 6 and 15 recite, "the reconfigurable logic device is a field programmable gate array device". It is unclear as to whether the "plurality of reconfigurable logic devices" in claims 1 and 11 are all intended to be field programmable gate array devices or if only one of the "plurality of reconfigurable logic devices" in claims 1 and 11 is a field programmable gate array device.

Claim Interpretation

15. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.

16. Claims 1 and 11 recite "each of the devices evenly connected to each of the other devices by wires in a complete graph interconnect structure". These limitations were interpreted according to the following statements in the specification: (page 3, line 35-page 4, line 7) "...To attain this, the present invention generally comprises a plurality of reconfigurable logic devices, such as field programmable gate array devices (FPGAs), having logic and interconnect elements which can be reconfigured for different functions, a "complete graph" interconnect structure having wires connecting all FPGAs together similar to a complete graph and having approximately equal number of wires between any pair of FPGAs", and (page 4, lines 18-22) "...The "complete graph" interconnect structure is characterized by every FPGA having all its connections evenly connected to the rest of FPGAs in the emulator. Therefore, direct connections exist between any pair of FPGAs".

17. Claim 6 recites, "the reconfigurable logic device is a field programmable gate array device". It is unclear as to whether the "plurality of reconfigurable logic devices" in claim 1 are all intended to be field programmable gate array devices or if only one of the "plurality of reconfigurable logic devices" in claim 1 is a field programmable gate array device. For the purposes of examination, the claim was interpreted to read as if all of the reconfigurable logic devices in claim 1 are field programmable logic devices.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

19. Claims 1-11, 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Khalid et al (US Patent 6,604,230).

20. As to Claims 1 and 11, Khalid et al teaches: a configurable hardware system comprising: a plurality of reconfigurable logic devices (column 5, lines 29-30), each of the devices evenly connected to each of the other devices by wires in a complete graph interconnect structure (column 8, lines 41-47), each of the devices capable of modeling a portion of an electronic circuit or system following configuration by a circuit coupled to the plurality of reconfigurable logic devices (column 6, lines 29-31; column 9, line 60-column 10, line 7; column 10, lines 44-48), the configuration based on partition of a design of the electronic circuit or system to be emulated (column 6, lines 56-66; column 9, line 60-column 10, line 7; column 10, lines 44-52; Figure 13, element 200) and including routing signals crossing each reconfigurable logic device's boundary (column 10, line 66-column 11, line 5) and assigning pins for each reconfigurable logic device (column 11, lines 10-24; column 8, lines 33-41).

21. As to Claims 2 and 11, Khalid et al teaches: software running on a host computer coupled to the plurality of reconfigurable logic devices that: a) imports into the system a design of the electronic circuit or system to be emulated (column 6, lines 29-31; column 9, line 60-column 10, line 7; column 10, lines 44-48); b) partitions the design among

individual reconfigurable logic devices within the limits of each device's logic and pin capacity, wherein the partition is constrained by a number of target pins for each reconfigurable logic device (column 9, line 60-column 10, line 7; column 10, lines 44-57; Figure 13, element 200); and c) produces a programming bitstream to configure each of the individual reconfigurable logic devices (column 10, line 63-column 11, line 2).

22. As to Claims 3 and 11, Khalid et al teaches: wherein the circuit performs at least one of the following functions: a) downloading the programming bitstream to configure each of the individual reconfigurable logic devices (column 10, line 63-column 11, line 2).

23. As to Claims 4 and 13, Khalid et al teaches: a user interface (column 10, lines 56-57, 63-65) wherein the "CAD Flow" is described in which inputs are applied to the program by a designer and a netlist is output. It is understood that a user interface is used in a CAD program, specifically wherein the designer will put parameters into the system and have means to view an output of the design.

24. As to Claims 5 and 14, Khalid et al teaches: each of the reconfigurable logic devices having wires for at least one of the following uses: e) interfacing with a target system (column 8, lines 48-63).

25. As to Claims 6 and 15, Khalid et al teaches: wherein the reconfigurable logic device is a field programmable gate array device (column 6, lines 31-39; column 2, lines 33-43).

26. As to Claims 7 and 16, Khalid et al teaches: the software giving a high priority for directly connecting timing-critical signals between two reconfigurable logic devices (column 11, lines 31-42).

27. As to Claims 8 and 17, Khalid et al teaches: wherein the software reserves pins on each reconfigurable logic device for signals between two reconfigurable logic devices which are routed through a third reconfigurable logic device (column 5, lines 52-58; column 8, lines 48-55).

28. As to Claims 9 and 18, Khalid et al teaches: wherein the software partitions the design to achieve a high target pin count for each reconfigurable logic device by routing fewer signals between a pair of reconfigurable devices through a third reconfigurable logic device (column 8, lines 41-47; column 8, line 64-column 9, line 13; column 9, lines 39-52).

29. As to Claims 10 and 19, Khalid et al teaches: a target system coupled to the plurality of reconfigurable logic devices (column 8, lines 48-63).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khalid et al as applied to claim 11 above, and further in view of Tseng et al (US Patent 6,009,256).

32. Khalid et al teaches the host computer software performing testing tasks (column 10, lines 11-15; column 12, lines 31-47).

33. Khalid et al does not expressly teach the host software performing debugging tasks.

34. Tseng et al teaches a flexible and fast simulation/emulation system that provides the speed of a hardware accelerator with the control of a software simulator (column 2, lines 41-47), and that in the typical test/debug scenario, reconfigurable devices are used to simulate/emulate the user's circuit design so that appropriate changes can be made prior to actual prototype manufacturing (column 13, lines 6-9) wherein the test/debug scenario, the user's circuit design is partitioned, mapped, placed and routed onto an array of FPGA chips (column 10, lines 1-6; column 12, lines 45-51) and includes the ability to switch between software simulation and hardware acceleration cycle-by-cycle, thereby allowing the user to go to a particular point or cycle very quickly using the

hardware acceleration mode and then using software simulation to examine various points thereafter to debug the design (column 12, lines 5-13).

35. Khalid et al and Tseng et al are analogous art since they are both directed to the partitioning, placement, routing and testing of a circuit design implemented on a plurality of FPGA chips.

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the host computer software performing testing tasks as taught by Khalid et al to further include debugging capabilities as taught by Tseng et al since Tseng et al teaches a flexible and fast simulation/emulation system that provides the speed of a hardware accelerator with the control of a software simulator (column 2, lines 41-47), and that in the typical test/debug scenario, reconfigurable devices are used to simulate/emulate the user's circuit design so that appropriate changes can be made prior to actual prototype manufacturing (column 13, lines 6-9).

Conclusion

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

38. Selvidge et al (US Patent 5,659,716) teaches a configurable logic system programmed to model a logic design comprises an array of programmable logic modules each configured to perform a partition block of the logic design and a module interconnect providing connections between the modules wherein the interconnect enables transmission of global links between the partition blocks of the modules.

39. Sample et al (US Patent 6,289,494) teaches a programmable logic device architecture that is particularly useful in logic emulation, prototyping and/or computing applications.

40. Sample et al (US Patent 5,644,515) teaches a system for physical emulation of electronic circuits or systems including a data entry workstation where a user may input data representing the circuit or system configuration. This data is converted to a form suitable for programming an array of programmable gate elements provided with a richly interconnected architecture.

41. Casselman (US Patent 5,684,980) teaches an array of FPGAs change their configurations successively during performance of successive user-defined algorithms. Adjacent FPGAs are connected through external field programmable interconnection devices (FPINs) or cross-bar switches.

42. Butts et al (US Patent 6,002,861) teaches a plurality of electronically reconfigurable gate array (ERCGA) logic chips are interconnected via a reconfigurable interconnect, and teaches the direct interconnect architecture.

43. Agarwal et al (US Patent 5,596,742) teaches a compilation technique to overcome device pin limitations using virtual interconnections.

44. Khalid et al ("A Novel and Efficient Routing Architecture for Multi-FPGA Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 1, February 2000) teaches a hybrid complete-graph and partial-crossbar routing architecture and teaches a router that tries to route all critical nets using direct connections.

45. Kim et al ("A Performance-Driven Logic Emulation System: FPGA Network Design and Performance-Driven Partitioning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 5, May 1996) teaches several architectures of FPGA networks, including the direct connect architecture, and compares them to other typical existing architectures.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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10/14/06

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